

CLAIMS

- 1 1. A circuit testing apparatus comprising:
 - 2 a controller for controlling signals being transferred between a circuit under
 - 3 test and the circuit testing apparatus; and
 - 4 a driver circuit for generating signals to be applied to the circuit under test,
 - 5 the driver circuit includes a high speed slave chain and a DC control loop chain
 - 6 coupled to the circuit under test, the high speed slave chain receives a differential
 - 7 voltage logic pulse train and converts said logic pulse train into an high speed
 - 8 current steering for producing said drive signal to be applied to the circuit under
 - 9 test, the DC control loop chain provides feedback paths for DC regulation of inputs
 - 10 of said high speed slave chain.
- 1 2. The circuit testing apparatus of claim 1, wherein the driver is a class A driver.
- 1 3. The circuit testing apparatus of claim 1, wherein the driver circuit is coupled to a
2 pin on the circuit under test.
- 1 4. The circuit testing apparatus of claim 1, further comprising a receiver circuit for
2 receiving output signals from the circuit under test.
- 1 5. The circuit testing apparatus of claim 4, wherein the receiver circuit is coupled to a
2 pin on the circuit under test.
- 1 6. The circuit testing apparatus of claim 4, wherein the receiver circuit and the driver
2 circuit are coupled together to a pin on the circuit under test.

- 1 7. The circuit testing apparatus of claim 1, wherein the high speed slave chain further
2 includes an input clamp stage for receiving said differential logic pulse train and
3 converting said differential logic pulse train into fixed amplitude complimentary
4 output voltages.
- 1 8. The circuit testing apparatus of claim 1, wherein the DC control loop chain further
2 includes an input clamp stage for receiving fixed differential logic signals and
3 converting said fixed differential logic pulse train into fixed amplitude
4 complimentary output voltages.
- 1 9. The circuit testing apparatus of claim 8, wherein the high speed slave chain and DC
2 control loop chain further include a current controlled gain stage for receiving fixed
3 amplitude complimentary output voltages of the input clamp stage and employing a
4 controlled cascode translinear multiplier cell configuration to provide a wide
5 bandwidth with high DC precision and low distortion means of controlling the
6 amplitude.
- 1 10. The circuit testing apparatus of claim 9, wherein the high speed slave chain and DC
2 control loop further includes an output stage that is a standard cascaded differential
3 linear amplifier.
- 1 11. The circuit testing apparatus of claim 10, wherein the output stage of the high speed
2 slave chain whose output currents drive an output resistor of the said driver.

- 1 12. The circuit testing apparatus of claim 10, wherein the output stage of DC control
2 loop chain provides feedback currents to DC control loop chain
- 1 13. The circuit testing apparatus of claim 1, wherein the high speed slave chain and DC
2 control loop chain further comprises an output stage that includes a differential-
3 input pair of transistors which receive a differential voltage input signal to drive the
4 their respective output stage circuits.
- 1 14. The circuit testing apparatus of claim 13, wherein the output stage further includes
2 a pair of transistors that receive a single-ended voltage input.
- 1 15. The circuit testing apparatus of claim 14, the output stage further includes a
2 resistance coupled between the transistors, the differential voltage input signal
3 controlling an amount of current through the resistance to control a current level in
4 each of the transistors to generate the drive signal applied to the circuit under test.
- 1 16. The circuit testing apparatus of claim 14, the output stage further includes a pair of
2 current sources coupled to the transistors, each of the current sources driving a
3 respective current through a respective one of the pair of transistors.
- 1 17. The circuit testing apparatus of claim 16, the output stage further includes a
2 resistance coupled between the transistors, the differential voltage input signal
3 controlling an amount of current through the resistance to control a current level in
4 each of the transistors to generate the drive signal applied to the circuit under test.

- 1 18. The circuit testing apparatus of claim 9, wherein the transistors are bipolar junction
2 transistors.
- 1 19. A circuit testing apparatus comprising:
2 controlling means for controlling signals being transferred between a circuit
3 under test and the circuit testing apparatus; and
1 driving means for generating signals to be applied to the circuit under test,
2 the driver circuit includes a high speed slave chain and a DC control loop chain
3 coupled to the circuit under test, the high speed chain circuit receives a differential
4 voltage logic pulse train and converts said logic pulse train into an high speed
5 current steering for producing said drive signal to be applied to the circuit under
6 test, the DC control loop chain provides feedback paths for DC regulation of inputs
7 of said high speed slave chain.
- 1 20. The circuit testing apparatus of claim 19, wherein the driver is a class A driver.
- 1 21. The circuit testing apparatus of claim 19, wherein the driver circuit is coupled to a
2 pin on the circuit under test.
- 1 22. The circuit testing apparatus of claim 19, further comprising a receiver circuit for
2 receiving output signals from the circuit under test.
- 1 23. The circuit testing apparatus of claim 22, wherein the receiver circuit is coupled to
2 a pin on the circuit under test.

- 1 24. The circuit testing apparatus of claim 22, wherein the receiver circuit and the driver
2 circuit are coupled together to a pin on the circuit under test.
- 1 25. The circuit testing apparatus of claim 19, wherein the high speed slave chain further
2 includes an input clamp stage for receiving said differential logic pulse train and
3 converting said differential logic pulse train into fixed amplitude complimentary
4 output voltages.
- 1 26. The circuit testing apparatus of claim 19, wherein the DC control loop chain further
2 includes an input clamp stage for receiving fixed differential logic signals and
3 converting said fixed differential logic pulse train into fixed amplitude
4 complimentary output voltages.
- 1 27. The circuit testing apparatus of claim 26, wherein the high speed slave chain and
2 DC control loop chain further include a current controlled gain stage for receiving
3 fixed amplitude complimentary output voltages of the input clamp stage and
4 employing a controlled cascode translinear multiplier cell configuration to provide
5 a wide bandwidth with high DC precision and low distortion means of controlling
6 the amplitude.
- 1 28. The circuit testing apparatus of claim 27, wherein the high speed slave chain and
2 DC control loop further includes an output stage that is a standard cascoded
3 differential linear amplifier.

- 1 29. The circuit testing apparatus of claim 28, wherein the output stage of the high speed
2 slave chain whose output currents drive an output resistor of the said driver.
- 1 30. The circuit testing apparatus of claim 29, wherein the output stage of DC control
2 loop chain provides feedback currents to DC control loop chain
- 1 31. The circuit testing apparatus of claim 19, wherein the high speed slave chain and
2 DC control loop chain further comprise an output stage that includes a differential-
3 input pair of transistors which receive a differential voltage input signal to drive the
4 their respective output stage circuits.
- 1 32. The circuit testing apparatus of claim 31, wherein the output stage further includes
2 a pair of transistors that receive a single-ended voltage input.
- 1 33. The circuit testing apparatus of claim 32, the output stage further includes a
2 resistance coupled between the transistors, the differential voltage input signal
3 controlling an amount of current through the resistance to control a current level in
4 each of the transistors to generate the drive signal applied to the circuit under test.
- 1 34. The circuit testing apparatus of claim 33, the output stage further includes a pair of
2 current sources coupled to the transistors, each of the current sources driving a
3 respective current through a respective one of the pair of transistors.
- 1 35. The circuit testing apparatus of claim 34, the output stage further includes a
2 resistance coupled between the transistors, the differential voltage input signal

3 controlling an amount of current through the resistance to control a current level in
4 each of the transistors to generate the drive signal applied to the circuit under test.

1 36. The circuit testing apparatus of claim 31, wherein the transistors are bipolar
2 junction transistors.

1 37. A method of testing a circuit, comprising:
2 providing a controller for controlling signals being transferred to and from
3 the circuit under test;
4 providing a driver circuit coupled to the circuit under test;
5 receiving a differential voltage logic pulse train; and
6 converting said logic pulse train into a high speed current steering for
7 producing said drive signal to be applied to the circuit under test.

1 38. The circuit testing apparatus of claim 37, wherein the driver circuit is a class A
2 driver.

1 39. The circuit testing apparatus of claim 37, wherein the driver circuit is coupled to a
2 pin on the circuit under test.

1 40. The circuit testing apparatus of claim 37, further providing a receiver circuit for
2 receiving output signals from the circuit under test.

1 41. The circuit testing apparatus of claim 40, wherein the receiver circuit is coupled to
2 a pin on the circuit under test.

- 1 42. The circuit testing apparatus of claim 41, wherein the receiver circuit and the driver
2 circuit are coupled together to a pin on the circuit under test.
- 1 43. The circuit testing apparatus of claim 38, wherein receiving said differential logic
2 pulse train further includes converting said differential logic pulse train into fixed
3 amplitude complimentary output voltages.
- 1 44. The circuit testing apparatus of claim 38, further comprising receiving fixed
2 differential logic signals and converting said fixed differential logic pulse train into
3 fixed amplitude complimentary output voltages.
- 1 45. The circuit testing apparatus of claim 44, further comprising receiving fixed
2 amplitude complimentary output voltages and employing a controlled cascode
3 translinear multiplier cell configuration to provide a wide bandwidth with high DC
4 precision and low distortion means of controlling the amplitude.
- 1 46. The circuit testing apparatus of claim 44, wherein the driver circuit further includes
2 a standard cascoded differential linear amplifier.